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(54) **Method for fabricating a liquid crystal display and display made by said method.**

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Description

Field of Invention

The present invention relates to a method for fabricating a liquid crystal display according to the preamble of claim 1 and to an active matrix liquid crystal display (AMLCD) achieved by said method as it is known from SID International Symposium Digest of Technical Papers. Vol. XX, 16 May 1989, Baltimore, US, pages 148-150; K.R. Sarma et al.: "Active-Matrix LCD's Using Gray-Scale in Halftone Methods".

Background of Invention

AMLCDs with a flat form factor have a demonstrated potential for reducing the weight, volume, power requirement, and cost, as well as for providing enhanced reliability compared to those factors of conventional cathode ray tube (CRT) displays. However, one significant problem with AMLCD panels has been the difficulty in achieving grayscale with adequate viewing angle. A number of display applications require wide-viewing angle grayscale and, without this, applications of AMLCD panels will be severely restricted.

In the above indicated document, a method for generating gray-scales in an AMLCD having a wide viewing angle and using a half-tone approach, already has been developed. Half-toning is accomplished by subdividing each pixel into a number of subpixels, and incorporating a control capacitor in series with each subpixel. The control capacitors act as voltage dividers. By using a proper choice of values for the control capacitors, the voltages across the subpixels are varied such that, as each subpixel is selected to be turned-on, the voltage across it is at or above saturation voltage, while the voltages across the unselected subpixels are at or below threshold voltage. For any gray level selected by varying the thin film transistor (TFT) source voltage, at the most, only one subpixel will be between the threshold voltage (V_{th}) and saturation voltage (V_s). This significantly reduces the viewing angle dependence of the pixel luminance and grayscale. The control capacitor capacitance that determines a particular voltage value of the selected pixel, is adjusted by variation in its area or thickness of the dielectric. In related art, the control capacitors and the active matrix array are fabricated at the same time on the same substrate.

One major problem with the related art approach is that design and processing trade-offs are required when fabricating an active matrix array having control capacitors on the same substrate. These trade-offs result in a detrimental effect on performance and yield. The active matrix substrate includes several thin films and processing steps. In the conventional active matrix substrate fabrication, the thin films, their thicknesses and the processing parameters are selected to optimize the performance and yield of the TFTs, and thus of the display. However, incorporation of control capacitors on the same substrate results in non-optimum film thicknesses or processing conditions for the TFT switching devices and/or the control capacitors.

The following instance illustrates a problem of related-art fabrication. The control capacitors, utilizing area variation as means for capacitance variation, require a second transparent conductive electrode, which is generally indium tin oxide (ITO). The second ITO layer is deposited after the TFT array fabrication is complete. For optimum ITO deposition conditions, the substrate will have to be heated in excess of 300° Centigrade (C). But this high temperature cycle degrades the properties of the a-Si TFTs.

To minimize the total number of process steps in fabrication, the TFT passivation layer is also used as a dielectric in the control capacitors with area variation. The choice of the dielectric and its thickness for the TFT passivation layer are determined by the dielectric/semiconductor interface properties and the step coverage issues. However, the choice of the dielectric and its thickness for the control capacitors is determined by the needed capacitance values for the control capacitors. These requirements of the dielectric and its thickness for TFTs and the control capacitors are usually not in agreement, and thus trade-offs need to be made if the same dielectric layer is to be used for TFT passivation as well as for control capacitors. Similarly, while the dielectric in the TFT structure can be used in the fabrication of control capacitors with thickness variation, the dielectric thickness requirements for the TFT structure and the control capacitors are quite different.

Another problem is that the conventional approach of the related art increases the number of processing steps (masking levels) for the TFT substrate. A greater number of steps increases the defect levels in the display and lowers the manufacturing yield. Negligible def ct levels and high manufacturing yields are essential for the success of AMLCD panels. So, becaus the yields and costs ar adversely affected as the number of masking levels and the process steps is increased, the related art requires design and process trade-offs to minimize the number of mask levels required for the fabrication of the active matrix substrates.

Accordingly, it is the object of the present invention to develop a method of manufacturing the half-tone grayscale displays with control capacitors that does not require design and process trade-offs with resulting performanc and yield degradation. This object is achieved by the characterizing features of claim 1. Further

advantageous embodiments of the inventive method may be taken from the dependent method claims. A liquid crystal display fabricated by the inventive method is subject of a further independent claim.

The present invention solves the object by separating the control capacitors from the active matrix substrate and having the active matrix substrate fabrication be strictly conventional. The control capacitors are fabricated on a second substrate containing the common electrode. The separation of the active matrix array and the control capacitor array between the two display glass substrates, permits each array to be fabricated with conventional techniques under its own optimum conditions to achieve high performance and yield, and low cost.

Summary of the Invention

The present invention is a structure and method of fabricating the active matrix displays with halftone grayscale and a wide viewing angle. In the related art, the subpixels are defined in the conventional active matrix. In the invention, the subpixels are defined by the common electrode substrate. The active matrix in the invention defines just the pixels. The invention includes separating the active matrix array from the control capacitor array. Splitting the fabrication and number of process steps between the active matrix substrate and the common electrode substrate, increases control over the manufacturing process, optimizes design parameters and permits noncritical, conventional fabrication.

Brief Description of the Drawings

Figure 1	is a graph revealing viewing angle dependence of transmission versus applied voltage of a typical twisted nematic liquid crystal display, with parallel polarizers.
Figure 2a	is a schematic of a related art pixel.
Figure 2b	is an electrical equivalent of the pixel in Figure 2a, according to the related art.
Figure 3a	is a schematic of the pixel as used in the present invention.
Figure 3b	is an electrical equivalent of the pixel in Figure 3a.
Figure 4	is a pattern of the common electrode substrate.
Figure 5	is the first ITO layer pattern in the fabrication of the common electrode substrate.
Figure 6	reveals the pattern in the dielectric layer for the control capacitors.
Figure 7	reveals the second ITO layer pattern in the fabrication of the common electrode substrate.
Figures 8a and 8b	show a cross-section through a TFT at a pixel and a plan view of the pixel and the TFT, respectively.
Figure 9	is a cross-section of liquid crystal material sandwiched between an active matrix substrate and a common electrode substrate, using spacers for maintaining desired cell spacing.
Figure 10	is a comparison of grayscale errors of the present invention and the conventional related art, for a 40 degree viewing angle.
Figure 11	shows an embodiment of the invention vith color filters.
Figure 12	shows an embodiment of the invention with variable-thickness, color filters for variable cell gap displays.
Figure 13	is a diagram outlining the method of fabrication.

Description of the Preferred Embodiments

Figure 1 is a graph revealing viewing angle dependence of transmission versus applied voltage of a typical twisted nematic liquid crystal display with parallel polarizers. The graph indicates the percent of transmission (T) of a pixel versus applied voltage for a viewing angle (Ø) of 0 and 20 degrees relative to the display normal. For voltage V_a, the transmission T_a for 0 degree viewing is about 45 percent and T_b for 20 degree viewing is about 80 percent. This results in a grayscale error of -78%,
i.e., ((45 - 80) / 45) x 100%. Large grayscale errors limit the viewing angle. Voltage corresponding to a transmission of 10% is taken as the threshold voltag (V_{th}), and the voltage corresponding to 90% transmission is taken as the saturation voltage (V_s).

Figure 2a is a diagram of related-art active matrix array 10. Figure 2b is a schematic of electrical equivalent 11 of the half-tone pixel in Figure 2a. Thin film transistors (TFTs) 15 and control capacitors 20 are both fabricated on substrate 13. Common electrode substrate 17 is merely the common conductor. Capacitors 19 represent the capacitances between substrates 13 and 17, which is a consequence of the liquid crystal display

pixels.

In the related art, there is a technique for generating grayscales in AMLCDs having a wide viewing angle, using a half-tone approach. The half-tone approach is based on the fact that the electro-optic response of liquid crystals is essentially independent of the viewing angle when the applied voltage is less than the threshold voltage, V_{th}, or greater than the saturation voltage, V_s, as illustrated in Figure 1.

The pixel half-toning is accomplished by subdividing each pixel into a number of subpixels, and incorporating a control capacitor in series with each subpixel as shown in Figure 2b. Control capacitors 20 and the active matrix array 10 are fabricated at the same time on same substrate 13. Control capacitors 20 act as voltage dividers. By using a proper choice of values for control capacitors 20, the voltages across the subpixels are varied such that, as each subpixel is selected to be turned-on, the voltage across it is at or above V_s, while the unselected pixels are at or below V_{th}. Thus, for any gray level selected by varying TFT 15 source voltage, at the most, only one subpixel voltage will be between V_{th} and V_s. This significantly reduces the pixel luminance and grayscale dependencies on viewing angle. The control capacitor 20 capacitance is varied by variation in capacitor area or thickness of the dielectric in substrate 13.

Figures 3a and 3b show a schematic of active matrix array 12 and electrical equivalent 14 of a pixel, according to the present invention. TFTs 15 and control capacitors 20 are fabricated on two separate substrates 16 and 18, respectively. Active matrix array 12 is fabricated on substrate 16 and control capacitor array 20 is fabricated on common electrode substrate 18. The fabrication of active matrix substrate 16 is conventional and thus can be designed and manufactured under optimum conditions for high performance and yield. Active matrix array 12 may be fabricated using a-Si TFTs, poly-Si TFTs or the like. Control capacitors 20 are fabricated on common electrode substrate 18 under optimum conditions for precise predetermined values of the control capacitor 20 capacitances and production yield.

Figure 4 shows the schematic of common electrode substrate 18. Each corresponding pixel is divided into four subpixels. An overlay of three thin film layers used to fabricate control capacitors 20 is revealed in Figure 4. Hatched portion 22 represents the first indium tin oxide (ITO) pattern on the common electrode substrate. First pattern 22 is separately illustrated in Figure 5. Plane pattern 24 indicates the second ITO pattern of series capacitors 20 on substrate 18. Pattern 24 is separately illustrated in Figure 7. Between patterns 22 and 24 is a dielectric of pattern 26 as illustrated in Figure 6.

A method of fabrication is shown in Figure 13. Substrate 18 is fabricated, starting with Corning 7059 glass, according to the following steps: 1) Sputter deposit 300 angstroms of indium tin oxide (ITO) at 300° C and anneal at 400° C, for 30 minutes. Photolithographically pattern and etch to define the area of control capacitors 20 as shown in Figure 5. Thus, this ITO 22 layer serves as a common electrode as well as to define the control capacitor 20 areas. 2) Plasma deposit 12,000 angstroms of silicon nitride dielectric. Photolithographically pattern and etch as shown in Figure 6. This pattern serves to remove a series control capacitor in one of the subpixels in the pixel. This subpixel will be the first one to turn-on, as the source voltage of the TFT is increased. 3) Sputter deposit a second ITO layer, 300 angstroms thick, at 300° C, and anneal at 400° C, for 30 minutes. Photolithographically pattern and etch to define the subpixels as shown in Figure 7. The above process completes the fabrication of control capacitors 20 on common electrode substrate 18.

Active matrix substrate 16 is fabricated conventionally under optimum conditions to obtain high process yields. An a-Si TFT with an inverted staggered structure is employed in the active matrix substrate 16 as shown in Figures 8a and 8b. Figure 8a shows a cross-section through the TFT at a pixel. Figure 8b shows the plan view of a pixel with the TFT. Substrate 16 is fabricated, starting with Corning 7059 glass 50, according to the following steps : 1) Sputter deposit 300 angstroms of indium tin oxide (ITO) at 300° C and anneal at 400° for thirty minutes. Let the substrate cool to 300° C, and sputter deposit 1200 angstroms of nichrome. Photolithographically pattern and etch the nichrome and the ITO to define pixels 54 and gate busses 51. 2) Deposit 3000 angstroms of silicon nitride and 1000 angstroms of amorphous silicon sequentially by plasma enhanced chemical vapor deposition (PECVD) at 250° C. Photolithographically pattern and etch the silicon nitride and the amorphous silicon to define transistor islands 52. 3) Sputter deposit 5000 angstroms of aluminum alloy (4% copper and 1% silicon). Photolithographically pattern and etch the aluminum alloy to define source 53 and drain 53. 4) Deposit 10,000 angstroms of silicon dioxide for a passivation layer by PECVD at 250° C. 5) Sputter deposit 1500 angstroms of aluminum alloy for a light shield. 6) Photolithographically pattern and etch light shield layer 56. 7) Photolithographically pattern and etch passivation layer 55 to clear pixels 54, and then etch the nichrome from pixels 54. Light shield layer 56 and passivation layer 55 are not shown in Figure 8b for the sake of clarity. The above process completes the fabrication of active matrix substrate 16.

Active matrix display 14 is then assembled as shown in Figure 9. Figure 9 shows liquid crystal material 64 sandwiched between active matrix substrate 16 and common electrode substrate 18, using spacers 65 to maintain the desired cell spacing. A MERCK 2861 liquid crystal material is employed in display 14 with a cell spacing of 4 microns. Liquid crystal alignment layer 61 on both substrates is created by a mechanically rubbed

polyimide layer. Polarizers 62 are attached to the outer surfaces of display 14 (i.e., th outer surfaces of substrates 16 and 18) in a parallel ori ntation.

Assembled display 14 is then tested for grayscale errors as a function of viewing angle. A substantial improvement in grayscale accuracy has been observed in halftone display 14 when compared to a conventional display. For instance, for a 40 degree viewing angle, the grayscale errors, as shown in Figure 10, were better than -50% for halftone display 14, whereas they were as high as -350% for a conventional display.

Figure 11 shows a cross-section of a completely fabricated common electrode substrate 30 of the invention, using color filters 32 for full-color operation. The cross-section reveals a common electrode substrate containing color filter array 32, as well as a control capacitor 20 array composing first ITO pattern 22, dielectric 26, and second ITO pattern 24, as set on glass substrate 34. The electrodes are part of pattern 24 and define the subpixels. Active matrix substrate 16 is registered with respect to pattern 24, during the display 14 assembly, with the liquid crystal material.

Figure 12 shows common electrode substrate 40 using color filters 36 with various thicknesses. The cross-section through the common electrode substrate is revealed. The thickness variation of color filters 36 results in a variation of the liquid crystal cell thickness for different colors for enhanced contrast. Other structural features of display 40 are like those of common electrode substrate 30.

It is thus seen from the foregoing that there is provided a structure and method for manufacturing wide viewing angle, active matrix displays with halftone grayscale with high performance, high manufacturing yield, and low cost. The foregoing detailed description is intended to be exemplary rather than limiting, and the description sets forth the best mode contemplated by the inventor of carrying out his invention.

Claims

1. A method of fabricating a wide viewing angle, active matrix liquid crystal display having pixels each divided into subpixels to provide a halftone grayscale capability,
comprising the steps of fabricating a control capacitor array on a first glass substrate,
fabricating an active matrix on a second glass substrate, juxtapositioning the control capacitor array on the first glass substrate next to the active matrix on the second glass substrate with a gap between, and filling the gap with a liquid crystal material,
wherein said fabricating the control capacitor array comprises:
depositing a first indium tin oxide layer on said first glass substrate;
annealing the indium tin oxide layer;
etching the first indium tin oxide layer according to a first pattern defining the pattern of the control capacitor array;
depositing a silicon nitride layer on the first indium tin oxide layer;
etching the silicon nitride layer according to a second pattern;
depositing a second indium tin oxide layer;
annealing the second indium tin oxide layer; and
etching the second indium tin oxide layer according to a third pattern so as to form separate areas each defining one of said subpixels;
and wherein said fabricating the active matrix comprises:
forming on said first substrate a plurality of transistors and an electrode layer divided into a plurality of areas each defining one of said pixels, and
connecting each of said transistors to a respective one of said pixel defining electrode areas.

2. Method according to claim 1,
wherein said sandwiching comprises:
using spacers placed between the capacitor array and the active matrix to maintain a cell spacing;
aligning the liquid crystal material on the first glass substrate and the second glass substrate through use of a rubbed-polyimide layer; and
attaching polarizers to outer surfaces of the first and second glass substrates.

3. Method according to claim 2,
wherein:
the liquid crystal material is MERCK 2861;
the first and second glass substrates are Corning 7059 glass; and
the etching of th first, second and third patterns is effected by photolithography.

4. Method according to claim 1,
wherein said fabricating the active matrix comprises:
sputter depositing an approximately 300 angstrom indium tin oxide layer at about 300 degrees Centigrade on said second glass substrate;
annealing the indium oxide layer at about 400 degrees Centigrade for about 30 minutes;
sputter depositing an approximately 1200 angstrom nichrome layer on the indium tin oxide layer;
making a first pattern on the nichrome layer and the indium tin oxide layer to define pixels and gate busses;
etching the first pattern;
plasma-enhanced-chemical-vapor depositing an approximately 3000 angstrom silicon nitride layer on the nichrome layer at about 250 degrees Centigrade;
plasma-enhanced-chemical-vapor depositing an approximately 1000 angstrom amorphous silicon layer on the silicon nitride layer at about 250 degrees Centigrade;
making a second pattern on the amorphous silicon layer and the silicon nitride layer to define islands for the thin film transistors;
etching the second pattern;
sputter depositing an approximately 5000 angstrom aluminum alloy layer on the amorphous layer;
making a third pattern on the aluminum alloy layer to define sources and drains for the thin film transistors;
etching the third pattern;
plasma-enhanced-chemical-vapor depositing an approximately 10,000 angstrom silicon dioxide passivation layer at about 250 degrees Centigrade on the aluminum alloy layer;
sputter depositing an approximately 1500 angstrom aluminum alloy light shield layer on the passivation layer;
making a fourth pattern on the light shield layer;
etching the fourth pattern;
making a fifth pattern on the passivation layer; and
etching the fifth pattern to clear the pixels of the passivation and nichrome layers.

5. A wide viewing angle, active matrix liquid crystal display arranged in the form of a plurality of pixels (12) each divided into subpixels to provide a halftone grayscale capability, comprising:
a first substrate (16) and a second substrate (18) with a liquid crystal material therebetween;
on said first substrate (16) a plurality of transistors (15) and an electrode layer divided into a plurality of areas each defining one of said pixels, wherein each of said transistors is connected to a respective one of said pixel defining electrode areas; and
a plurality of control capacitor groups (20), wherein the first electrodes of each control capacitor within each group have a common connection by consisting of a common electrode layer, and the second electrodes of said control capacitors consist of separate electrode areas each defining one of said subpixels such that each control capacitor is connected in series to the capacitance of the liquid crystal material corresponding to the respective subpixel and such that each control capacitor group corresponds to one of said pixels;
characterized in that
said plurality of control capacitor groups (20) is provided on said second substrate (18).

6. Liquid crystal display according to claim 5,
characterized in that said second substrate comprises:
a first glass substrate (18) with:
a first layer of indium tin oxide deposited on said first glass substrate (18) and having an etched pattern (22) that defines an area for said control capacitors (20) and serving as said common electrode layer for the control capacitors (20);
a first layer of silicon nitride dielectric deposited on said first layer of indium tin oxide (22), having an etched pattern (26) that defines the dielectric for the control capacitors (20);
a second layer of indium tin oxide (24) deposited on said first layer of silicon nitride dielectric (22), having an etched pattern that defines areas for said subpixels; and
a first alignment layer (61) of polyimide deposited on said second layer of indium tin oxide.

7. Liquid crystal display according to claim 6,
characterized by filters (32, 36) inserted between said first glass substrate (18) and said first layer of indium tin oxide (22), for full color operation.

8. Liquid crystal display according to claim 7,
charact riz d in that said color filters (32, 36) have varied thicknesses for enhancing contrasts of said display.

9. Liquid crystal display according to claim 6,
characterized in that said first substrate comprises a second glass substrate (16) with:
a third layer of indium tin oxide deposited on said second glass substrate (16);
a layer of nichrome deposited on said third layer of indium tin oxide, wherein said third layer of indium tin oxide and said layer of nichrome have an etched pattern that defines pixels (54), transistor gates and gate busses (51);
a second layer of silicon nitride deposited on said layer of nichrome;
a layer of amorphous silicon deposited on said second layer of silicon nitride, wherein said second layer of silicon nitride and said layer of amorphous silicon have an etched pattern that defines transistor islands (52);
a first layer of aluminum alloy deposited on said second layer of silicon nitride and layer of amorphous silicon, having an etched pattern defining transistor sources (53) and drains (53);
a passivation layer (55) of silicon dioxide deposited on said first layer of aluminum alloy;
a second layer of aluminum alloy deposited on said passivation layer (55), having an etched pattern defining a light shield (56), wherein said passivation layer (55) has an etched pattern clearing the pixels (54) of said passivation layer (55) and said layer of nichrome;
a second alignment layer of polyimide deposited on said third layer of indium tin oxide; and
a layer of liquid crystal material (64) sandwiched between said first and second alignment layers of polyimide, resulting in said active matrix liquid crystal display.

10. Liquid crystal display according to claim 9,
characterized by:
spacers (65) situated between said first and second substrates to maintain desired spacing;
a first layer of polarization material (62) attached to said first substrate (18); and
a second layer of polarization material (62) attached to said second substrate (16).

11. Liquid crystal display according to claim 10,
characterized in that:
said first layer of indium tin oxide is about 300 angstroms thick;
said first silicon nitride dielectric is about 12,000 angstroms thick;
said second layer of indium tin oxide is about 300 angstroms thick;
said third layer of indium tin oxide is about 300 angstroms thick;
said layer of nichrome is about 1200 angstroms thick;
said second layer of silicon nitride is about 3000 angstroms thick;
said layer of amorphous silicon is about 1000 angstroms thick;
said first layer of aluminum alloy is about 5000 angstroms thick;
said passivation layer is about 10,000 angstroms thick; and
said second layer of aluminum alloy is about 1500 angstroms thick.

12. Liquid crystal display according to claim 9,
characterized in that said aluminium alloy contains 4 percent copper and 1 percent silicon.

Patentansprüche

1. Verfahren zur Herstellung einer aktiven Matrix-Weitwinkel-Flüssigkristallanzeige mit Pixeln, die jeweils in Subpixel unterteilt sind, um die Möglichkeit eines Halbton-Graupegels vorzugeben, umfassend die Schritte der Herstellung einer Steuerkondensatoranordnung auf einem ersten Glassubstrat,
Herstellung einer aktiven Matrix auf einem zweiten Glassubstrat,
Nebeneinanderanordnung der Steuerkondensatoranordnung auf dem ersten Glassubstrat in der Nähe der aktiven Matrix auf dem zweiten Glassubstrat mit einer Lücke dazwischen und Füllen der Lücke mit einem Flüssigkristallmaterial,wobei di Herstellung der Steuerkondensatoranordnung umfaßt:
Ablagerung einer ersten Indium/Zinnoxydschicht auf dem ersten Glassubstrat;
Ausglühen der Indium/Zinnoxydschicht;

Ätzen der ersten Indium/Zinnoxydschicht gemäß einem ersten Muster, das das Muster der Steuerkondensatoranordnung definiert;
Ablagerung einer Silicium/Nitridschicht auf der ersten Indium/Zinnoxydschicht;
Ätzen der Silicium/Nitridschicht gemäß einem zweiten Muster;
Ablagerung einer zweiten Indium/Zinnoxydschicht;
Ausglühen der zweiten Indium/Zinnoxydschicht; und
Ätzen der zweiten Indium/Zinnoxydschicht gemäß einem dritten Muster, um getrennte Bereiche zu bilden, von denen jeder eines der Subpixel definiert;
und wobei die Herstellung der aktiven Matrix umfaßt:
Bildung mehrerer Transistoren und einer in mehrere Bereiche unterteilten Elektrodenschicht auf dem ersten Substrat, wobei jeder Bereich ein Pixel definiert, und
Verbindung eines jeden Transistors mit einem entsprechenden das Pixel definierenden Elektrodenbereich.

2. Verfahren nach Anspruch 1, **dadurch gekennzeichnet**, daß die Überlagerung umfaßt:
die Verwendung von Abstandshaltern zwischen der Kondensatoranordnung und der aktiven Matrix, um einen Zellenabstand aufrechtzuerhalten;
die Ausrichtung des Flüssigkristallmaterials auf dem ersten Glassubstrat und dem zweiten Glassubstrat durch die Verwendung einer aufgeriebenen Polyimidschicht; und
die Anbringung von Polarisatoren auf den Außenflächen der ersten und zweiten Glassubstrate.

3. Verfahren nach Anspruch 2, **dadurch gekennzeichnet**, daß
das Flüssigkristallmaterial durch MERCK 2861 vorgegeben ist;
die ersten und zweiten Glassubstrate aus Corning 7059 bestehen; und
das Ätzen der ersten, zweiten und dritten Muster photolithographisch erfolgt.

4. Verfahren nach Anspruch 1, **dadurch gekennzeichnet**, daß die Herstellung der aktiven Matrix umfaßt:
die Ablagerung durch Zerstäubung einer Indium/Zinnoxydschicht von ungefähr 300 Å bei ungefähr 300°C auf dem zweiten Glassubstrat;
das Ausglühen der Indiumoxydschicht bei ungefähr 400°C während ungefähr 30 Minuten;
die Ablagerung durch Zerstäuben von einer Nickel/Chromschicht von ungefähr 1200 Å auf der Indium/Zinnoxydschicht;
die Herstellung eines ersten Musters auf der Nickel-/Chromschicht und der Indium/Zinnoxydschicht, um Pixel und Steuerelektrodenbusse zu definieren;
das Ätzen des ersten Musters;
eine durch Plasma verbesserte chemische Dampfablagerung einer Silicium/Nitridschicht von ungefähr 3000 Å auf der Nickel/Chromschicht bei ungefähr 250°C;
eine durch Plasma verbesserte chemische Dampfablagerung einer amorphen Siliciumschicht von ungefähr 1000 Å auf der Silicium/Nitridschicht bei ungefähr 250°C;
die Herstellung eines zweiten Musters auf der amorphen Siliciumschicht und der Silicium/Nitridschicht, um Inseln für die Dünnfilmtransistoren zu definieren;
das Ätzen des zweiten Musters;
Die Ablagerung durch Zerstäubung einer Aluminium-Legierungsschicht von ungefähr 5000 Å auf der amorphen Schicht;
die Herstellung eines dritten Musters auf der Aluminium-Legierungsschicht, um Quellen und Senken für die Dünnfilmtransistoren zu definieren;
das Ätzen des dritten Musters;
eine durch Plasma verbesserte chemische Dampfablagerung einer Siliciumdioxyd-Passivierungsschicht von ungefähr 10.000 Å bei ungefähr 250°C auf der Aluminium-Legierungsschicht;
die Ablagerung durch Zerstäubung einer Aluminium-Legierungs-Lichtabschirmungsschicht von ungefähr 1500 Å auf der Passivierungsschicht;
die Herstellung eines vierten Musters auf der Lichtabschirmungsschicht;
das Ätzen der vierten Schicht;
die Herstellung eines fünften Musters auf der Passivierungsschicht; und
das Ätzen des fünften Musters, um die Pixel von der Passivierungsschicht und den Nickel/Chromschichten zu befreien.

5. Eine aktive Matrix-Weitwinkel-Flüssigkristallanzeige, die in der Form mehrerer Pixel (12) angeordnet ist,

welche jeweils in Subpixel unterteilt sind, um die Möglichkeit eines Halbton-Graupegels vorzugeben, g - k nnzeichnet durch
ein erstes Substrat (16) und ein zweites Substrat (18) mit einem Flüssigkristallmaterial dazwischen;
mehrere Transistoren (15) und eine in mehrere Bereiche unterteilte Elektrodenschicht auf dem ersten Substrat (16), wobei jeder Bereich ein Pixel definiert und wobei jeder Transistor an einen entsprechenden ein Pixel definierenden Elektrodenbereich angeschlossen ist; und
mehrere Steuerkondensatorgruppen (20), wobei die ersten Elektroden eines jeden Steuerkondensators innerhalb jeder Gruppe eine gemeinsame Verbindung besitzen, die aus einer gemeinsamen Elektrodenschicht besteht, und die zweiten Elektroden der Steuerkondensatoren aus getrennten Elektrodenbereichen bestehen, die jeweils eines der Subpixel definieren, so daß jeder Steuerkondensator in Reihe zu der Kapazität des Flüssigkristallmaterials geschaltet ist, die zu dem entsprechenden Subpixel gehört und so daß jede Steuerkondensatorgruppe zu einem der Pixel gehört;
dadurch gekennzeichnet, daß
die mehreren Steuerkondensatorgruppen (20) auf dem zweiten Substrat (18) angeordnet sind.

6. Flüssigkristallanzeige nach Anspruch 5,
dadurch gekennzeichnet, daß das zweite Substrat umfaßt:
ein erstes Glassubstrat (18) mit:
einer ersten Schicht aus Indium/Zinnoxyd, die auf dem ersten Glassubstrat (18) abgelagert ist und ein geätztes Muster (22) aufweist, das einen Bereich für die Steuerkondensatoren (20) definiert und als die gemeinsame Elektrodenschicht für die Steuerkondensatoren (20) dient;
einer ersten Schicht aus Silicium/Nitrid-Dielektrikum, das auf der ersten Schicht von Indium/Zinnoxyd (22) abgelagert ist und ein geätztes Muster (26) aufweist, das das Dielektrikum für die Steuerkondensatoren (20) definiert;
einer zweiten Schicht aus Indium/Zinnoxyd (24), die auf der ersten Schicht aus Silicium/Nitrid-Dielektrikum (22) abgelagert ist und ein geätztes Muster aufweist, das Bereiche für die Subpixel definiert; und
einer ersten Ausrichtschicht (61) aus Polyimid, die auf der zweiten Schicht aus Indium/Zinnoxyd abgelagert ist.

7. Flüssigkristallanzeige nach Anspruch 6,
gekennzeichnet durch Filter (32,36), die zwischen dem ersten Glassubstrat (18) und der ersten Schicht aus Indium/Zinnoxyd (22) für einen Voll-Farbenbetrieb eingesetzt sind.

8. Flüssigkristallanzeige nach Anspruch 7,
dadurch gekennzeichnet, daß die Farbfilter (32,36) unterschiedliche Dicken für die Verbesserung des Anzeigekontrasts aufweisen.

9. Flüssigkristallanzeige nach Anspruch 6,
dadurch gekennzeichnet, daß das erste Substrat ein zweites Glassubstrat (16) umfaßt mit:
einer dritten Schicht aus Indium/Zinnoxyd, die auf dem zweiten Glassubstrat (16) abgelagert ist;
einer Schicht aus Nickel/Chrom, die auf der dritten Schicht von Indium/Zinnoxyd abgelagert ist, wobei die dritte Schicht aus Indium/Zinnoxyd und die Schicht aus Nickel/Chrom ein geätztes Muster besitzt und Pixel (54), Transistor-Steuerelektroden und Steuerelektrodenbusse (51) definiert;
einer zweiten Schicht aus Siliciumnitrid, die auf der Schicht aus Nickel/Chrom abgelagert ist;
einer Schicht aus amorphem Silicium, die auf der zweiten Schicht von Siliciumnitrid abgelagert ist, wobei die zweite Schicht aus Siliciumnitrid und die Schicht aus amorphem Silicium ein geätztes Muster aufweisen, das Transistorinseln (52) definiert;
einer ersten Schicht aus Aluminiumlegierung, die auf der zweiten Schicht von Siliciumnitrid und der Schicht aus amorphem Silicium abgelagert ist und ein geätztes Muster besitzt, das Transistorquellen (53) und Senken (53) definiert;
einer Passivierungsschicht (55) aus Siliciumdioxyd, die auf der ersten Schicht aus Aluminiumlegierung abgelagert ist;
einer zweiten Schicht aus Aluminiumlegierung, die auf der Passivierungsschicht (55) abgelagert ist und ein geätztes Muster besitzt, das eine Lichtabschirmung (56) definiert, wobei die Passivierungsschicht (55) ein geätztes Muster besitzt, das die Pixel (54) von der Passivierungsschicht (55) und von der Schicht aus Nickel/Chrom befreit;
einer zweiten Ausrichtschicht aus Polyimid, di auf der dritten Schicht aus Indium/Zinnoxyd abgelagert ist; und

einer Schicht aus Flüssigkristallmaterial (64), eingebettet zwischen die ersten und zweiten Ausrichtschichten aus Polyimid, was zu einer aktiven Matrix-Flüssigkristallanzeige führt.

10. Flüssigkristallanzeige nach Anspruch 9,
gekennzeichnet durch:
Abstandsstücke (65), die zwischen den ersten und zweiten Substraten angeordnet sind, um den gewünschten Abstand aufrechtzuerhalten;
eine erste Schicht aus Polarisationsmaterial (62), die mit dem ersten Substrat (18) verbunden ist; und
eine zweite Schicht aus Polarisationsmaterial (62), die mit dem zweiten Substrat (16) verbunden ist.

11. Flüssigkristallanzeige nach Anspruch 10,
dadurch gekennzeichnet, daß:
die erste Schicht aus Indium/Zinnoxyd ungefähr 300 Å dick ist;
das erste Silicium/Nitrid-Dielektrikum ungefähr 12.000 Å dick ist;
die zweite Schicht aus Indium/Zinnoxyd ungefähr 300 Å dick ist;
die dritte Schicht aus Indium/Zinnoxyd ungefähr 300 Å dick ist;
die Schicht aus Nickel/Chrom ungefähr 1200 Å dick ist;
die zweite Schicht aus Siliciumnitrid ungefähr 3000 Å dick ist;
die Schicht aus amorphem Silicium ungefähr 1000 Å dick ist;
die erste Schicht aus der Aluminiumlegierung ungefähr 5000 Å dick ist;
die Passivierungsschicht ungefähr 10.000 Å dick ist; und
die zweite Schicht aus der Aluminiumlegierung ungefähr 1500 Å dick ist.

12. Flüssigkristallanzeige nach Anspruch 9,
dadurch gekennzeichnet, daß die Aluminiumlegierung 4% Kupfer und 1% Silicium enthält.

Revendications

1. Procédé de fabrication d'un afficheur à cristal liquide, à matrice active et angle d'observation étendu, ayant des pixels divisés chacun en des sous-pixels afin de fournir une capacité d'échelle de gris à demi-teintes,
comprenant les étapes consistant à fabriquer un réseau de condensateurs de commande sur un premier substrat en verre
fabriquer une matrice active sur un second substrat en verre,
juxtaposer le réseau de condensateurs de commande sur le premier substrat en verre à côté de la matrice active sur le second substrat en verre avec un intervalle entre eux, et
remplir l'intervalle avec un matériau de cristal liquide,
dans lequel ladite fabrication du réseau de condensateurs de commande comprend:
un dépôt d'une première couche d'oxyde d'étain et d'indium sur ledit premier substrat en verre;
une recuisson de la couche d'oxyde d'étain et d'indium;
une gravure de la première couche d'oxyde d'étain et d'indium conformément à un premier motif définissant le motif du réseau de condensateurs de commande;
un dépôt d'une couche de nitrure de silicium sur la première couche d'oxyde d'étain et d'indium;
une gravure de la couche de nitrure de silicium conformément à un second motif;
un dépôt d'une seconde couche d'oxyde d'étain et d'indium;
une recuisson de la seconde couche d'oxyde d'étain et d'indium; et
une gravure de la seconde couche d'oxyde d'étain et d'indium conformément à un troisième motif afin de former des zones séparées définissant chacune l'un desdits sous-pixels;
et dans lequel ladite fabrication de la matrice active comprend:
une formation sur ledit premier substrat d'une pluralité de transistors et d'une couche d'électrode divisée en une pluralité de zones définissant chacune l'un desdits pixels, et
une connexion de chacun desdits transistors à l'une respective desdites zones d'électrode de définition de pixel.

2. Procédé selon la revendication 1, dans lequel ladite fabrication en sandwich comprend:
une utilisation d'éléments d'écartement placés entre le réseau de condensateurs et la matrice active afin de maintenir un écartement de cellule;

un alignement du matériau de cristal liquid sur le premier substrat en verre et le second substrat en verre à travers l'utilisation d'une couche de polyimide au caoutchouc; et

une fixation de polariseurs aux des surfaces externes des premier et second substrats en verre.

3. Procédé selon la revendication 2, dans lequel:

le matériau de cristal liquide est du MERCK 2861;

les premier et second substrats en verre sont en verre Corning 7059; et

la gravure des premier, second et troisième motifs est effectuée par photolithographie.

4. Procédé selon la revendication 1, dans lequel ladite fabrication de la matrice active comprend:

un dépôt par pulvérisation cathodique d'une couche d'oxyde d'étain et d'indium d'approximativement 300 angstroems à environ 300 degrés centigrades sur ledit second substrat en verre;

une recuisson de la couche d'oxyde d'étain et d'indium à environ 400 degrés centigrades pendant environ 30 minutes;

un dépôt par pulvérisation cathodique d'une couche de nichrome d'approximativement 1200 angstroems sur la couche d'oxyde d'étain et d'indium;

une réalisation d'un premier motif sur la couche de nichrome et la couche d'oxyde d'étain et d'indium afin de définir des pixels et des bus de grille;

une gravure du premier motif;

un dépôt chimique en phase vapeur enrichi au plasma d'une couche de nitrure de silicium d'approximativement 3000 angstroems sur la couche de nichrome à environ 250 degrés centigrades;

un dépôt chimique en phase vapeur enrichi au plasma d'une couche de silicium amorphe d'approximativement 1000 angstroems sur la couche de nitrure de silicium à environ 250 degrés centigrades;

une réalisation d'un second motif sur la couche de silicium amorphe et la couche de nitrure de silicium afin de définir des îlots pour les transistors à couche mince;

une gravure du second motif;

un dépôt par pulvérisation cathodique d'une couche d'alliage d'aluminium d'approximativement 5000 angstroems sur la couche amorphe;

une réalisation d'un troisième motif sur la couche d'alliage d'aluminium afin de définir des sources et des drains pour les transistors à couche mince;

une gravure du troisième motif;

un dépôt chimique en phase vapeur enrichi au plasma d'une couche de passivation de dioxyde de silicium d'approximativement 10000 angstroems à environ 250 degrés centigrades sur la couche d'alliage d'aluminium;

un dépôt par pulvérisation cathodique d'une couche de protection contre la lumière en alliage d'aluminium d'approximativement 1500 angstroems sur la couche de passivation;

une réalisation d'un quatrième motif sur la couche de protection contre la lumière;

une gravure du quatrième motif;

une réalisation d'un cinquième motif sur la couche de passivation; et

une gravure d'un cinquième motif pour dégager les pixels des couches de passivation et de nichrome.

5. Afficheur à cristal liquide, à matrice active et angle d'observation étendu, configuré sous la forme d'une pluralité de pixels (12) divisés chacun en des sous-pixels afin de fournir une capacité d'échelle de gris à demi-teintes, comprenant:

un premier substrat (16) et un second substrat (18) avec un matériau de cristal liquide disposé entre eux;

sur ledit premier substrat (16), une pluralité de transistors (15) et une couche d'électrode divisée en une pluralité de zones définissant chacune l'un desdits pixels, dans lequel chacun desdits transistors est connecté à l'une respective desdites zones d'électrode de définition de pixel; et

une pluralité de groupes de condensateurs de commande (20), dans lequel les premières électrodes de chaque condensateur de commande dans chaque groupe ont une connexion commune consistant en une couche d'électrode commune, et les secondes électrodes desdits condensateurs de commande sont constituées de zones d'électrode séparées définissant chacune l'un desdits sous-pixels de telle façon que chaque condensateur de commande est connecté en série à la capacité du matériau de cristal liquide correspondant au sous-pixel respectif et de telle façon que chaque groupe de condensateurs de commande correspond à l'un desdits pixels; caractérisé en ce que ladite pluralité de groupes de condensateurs de commande (20) est prévue sur ledit second substrat (18).

6. Afficheur à cristal liquide selon la revendication 5, caractérisé en ce que ledit second substrat comprend:
un premier substrat en verre (18) avec:
une première couche d'oxyde d'étain et d'indium déposée sur ledit premier substrat en verre (18) et ayant un motif gravé (22) qui définit une zone pour lesdits condensateurs de commande (20) et utilisée en tant que ladite couche d'électrode commune pour les condensateurs de commande (20);
une première couche de diélectrique de nitrure de silicium déposée sur ladite première couche d'oxyde d'étain et d'indium (22), ayant un motif gravé (26) qui définit le diélectrique pour les condensateurs de commande (20);
une seconde couche d'oxyde d'étain et d'indium (24) déposée sur ladite première couche de diélectrique de nitrure de silicium (22), ayant un motif gravé qui définit des zones pour lesdits sous-pixels; et une première couche d'alignement (61) de polyimide déposée sur ladite seconde couche d'oxyde d'étain et d'indium.

7. Afficheur à cristal liquide selon la revendication 6, caractérisé par des filtres (32, 36) insérés entre ledit premier substrat en verre (18) et ladite première couche d'oxyde d'étain et d'indium (22), pour un fonctionnement en couleurs intégrales.

8. Afficheur à cristal liquide selon la revendication 7, caractérisé en ce que lesdits filtres de couleur (32, 36) ont des épaisseurs variées afin d'améliorer les contrastes dudit afficheur.

9. Afficheur à cristal liquide selon la revendication 6, caractérisé en ce que ledit premier substrat comprend un second substrat en verre (16) avec:
une troisième couche d'oxyde d'étain et d'indium déposée sur ledit second substrat en verre (16);
une couche de nichrome déposée sur ladite troisième couche d'oxyde d'étain et d'indium, dans lequel ladite troisième couche d'oxyde d'étain et d'indium et ladite couche de nichrome comprennent un motif gravé qui définit des pixels (54), des grilles de transistor et des bus de grille (51);
une seconde couche de nitrure de silicium déposée sur ladite couche de nichrome;
une couche de silicium amorphe déposée sur ladite seconde couche de nitrure de silicium, dans lequel ladite seconde couche de nitrure de silicium et ladite couche de silicium amorphe comprennent un motif gravé qui définit des îlots de transistor (52);
une première couche d'alliage d'aluminium déposée sur lesdites seconde couche de nitrure de silicium et couche de silicium amorphe, ayant un motif gravé définissant des sources (53) et des drains (53) de transistors;
une couche de passivation (55) de dioxyde de silicium déposée sur ladite première couche d'alliage d'aluminium;
une seconde couche d'alliage d'aluminium déposée sur ladite couche de passivation (55), ayant un motif gravé définissant un écran de protection contre la lumière (56), dans lequel ladite couche de passivation (55) comprend un motif gravé dégageant les pixels (54) de ladite couche de passivation (55) et ladite couche de nichrome;
une seconde couche d'alignement de polyimide déposée sur ladite troisième couche d'oxyde d'étain et d'indium; et
une couche en matériau de cristal liquide (64) intercalée entre lesdites première et seconde couches d'alignement de polyimide, ce qui donne ledit afficheur à cristal liquide à matrice active.

10. Afficheur à cristal liquide selon la revendication 9, caractérisé par:
des éléments d'écartement (65) situés entre lesdits premier et second substrats afin de maintenir l'écartement désiré;
une première couche de matériau de polarisation (62) fixée audit premier substrat (18); et
une seconde couche de matériau de polarisation (62) fixée audit second substrat (16).

11. Afficheur à cristal liquide selon la revendication 10, caractérisé en ce que:
ladite première couche d'oxyde d'étain et d'indium a environ 300 angstroems d'épaisseur;
ledit premier diélectrique de nitrure de silicium a environ 12000 angstroems d'épaisseur;
ladite seconde couche d'oxyde d'étain et d'indium a environ 300 angstroems d'épaisseur;
ladite troisième couche d'oxyde d'étain et d'indium a environ 300 angstroems d'épaisseur;
ladite couche de nichrome a environ 1200 angstroems d'épaisseur;
ladit seconde couche de nitrure de silicium a environ 3000 angstroems d'épaisseur;
ladite couche de silicium amorphe a environ 1000 angstroems d'épaisseur;

ladite première couche d'alliage d'aluminium a environ 5000 angstroems d'épaisseur;
ladite couche de passivation a environ 10000 angstroems d'épaisseur; et
ladite seconde couche d'alliage d'aluminium a environ 1500 angstroems d'épaisseur.

12. Afficheur à cristal liquide selon la revendication 9, caractérisé en ce que ledit alliage d'aluminium contient 4 pour-cent de cuivre et 1 pour-cent de silicium.

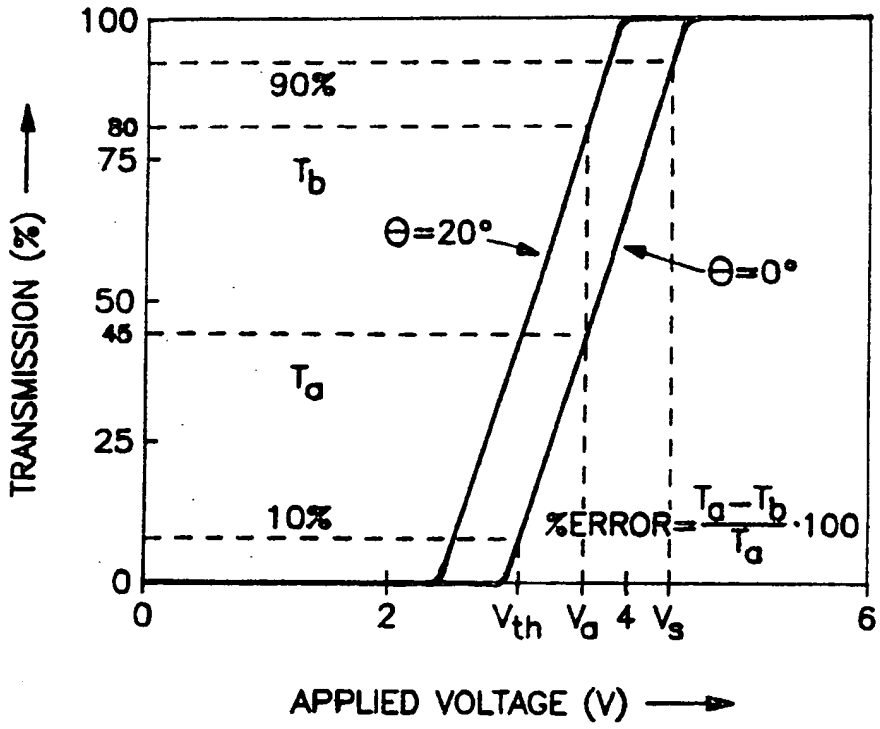
100
90%
80
75
T_b
Θ=20°
Θ=0°
50
45
T_a
25
10%
0
%ERROR=$\frac{T_a-T_b}{T_a}\cdot 100$
0
2
V_{th}
V_a
4
V_s
6
TRANSMISSION (%)
APPLIED VOLTAGE (V)

Fig. 1

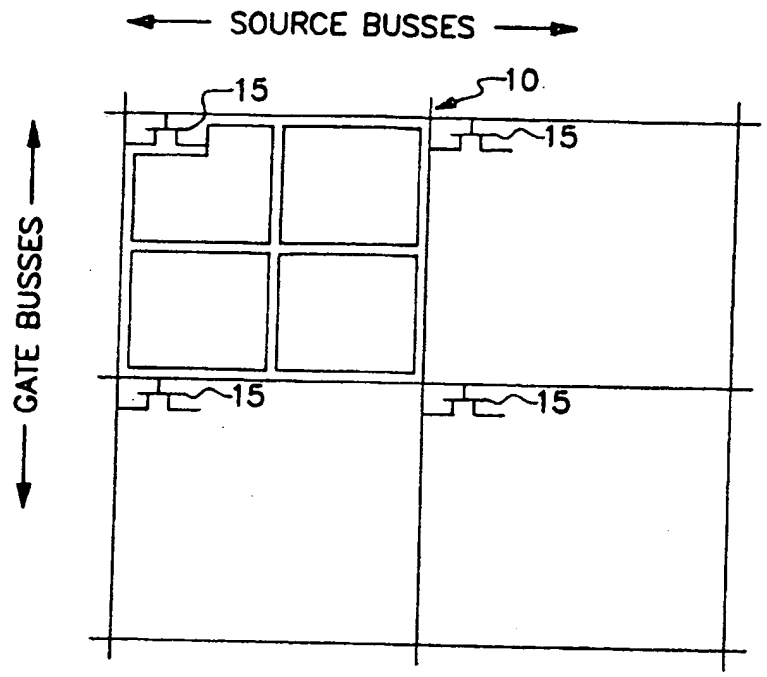
SOURCE BUSSES
GATE BUSSES
15
10
15
15
15

Fig. 2a

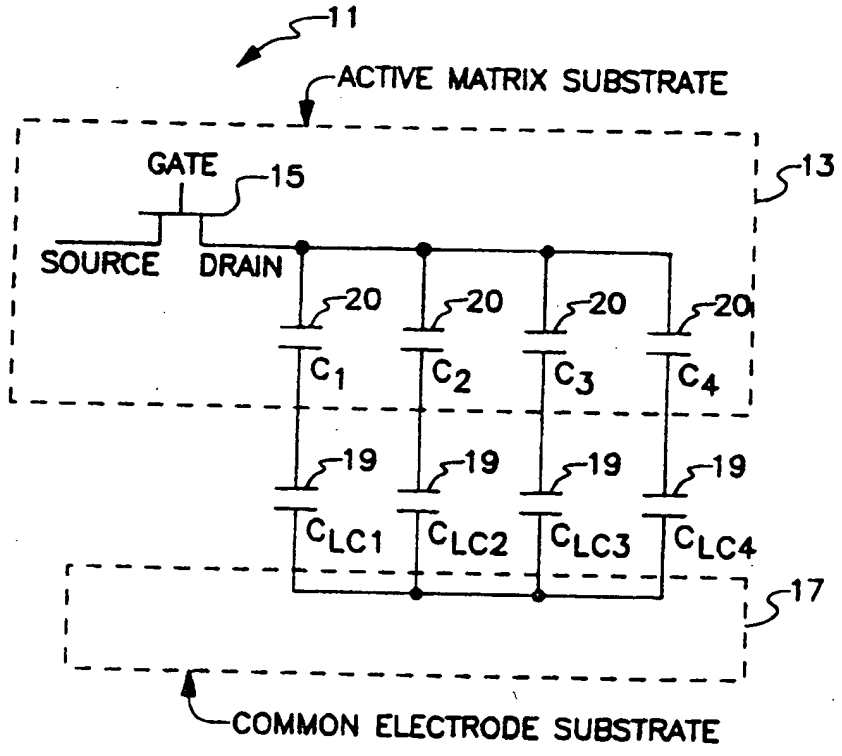
11
ACTIVE MATRIX SUBSTRATE
GATE
15
13
SOURCE
DRAIN
20
20
20
20
C1
C2
C3
C4
19
19
19
19
CLC1
CLC2
CLC3
CLC4
17
COMMON ELECTRODE SUBSTRATE

Fig. 2b

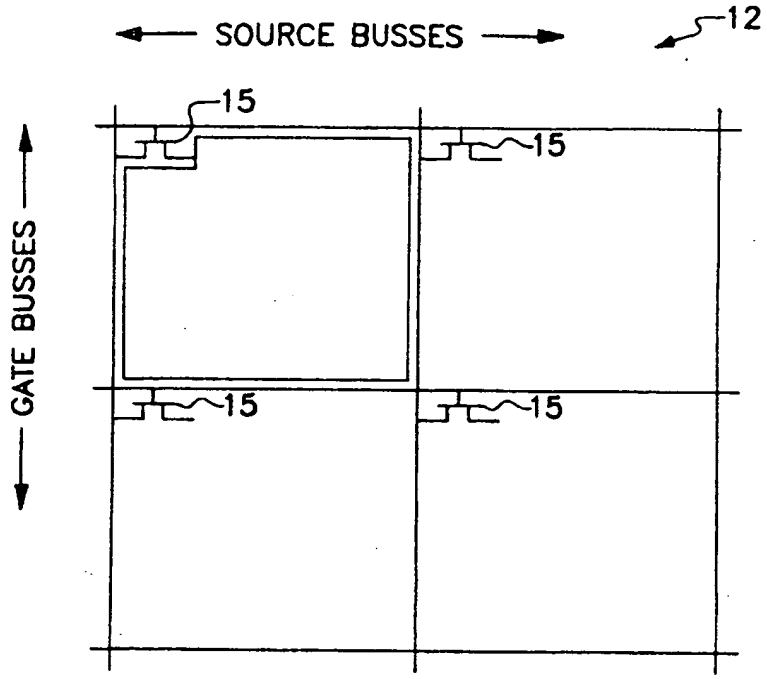
SOURCE BUSSES
12
15
15
15
15
GATE BUSSES

Fig. 3a

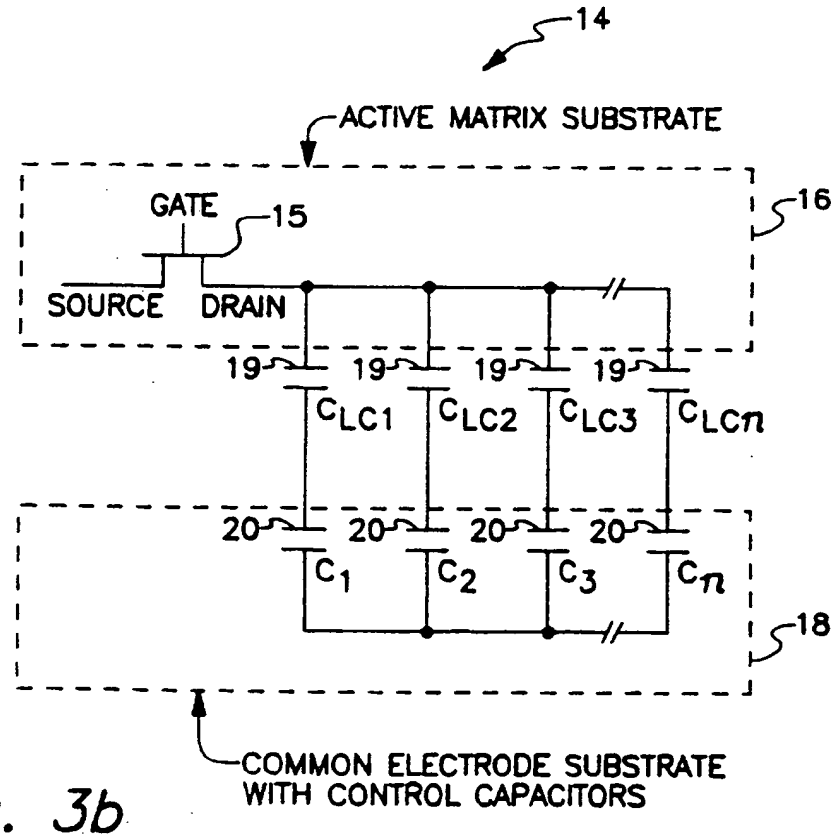
14
ACTIVE MATRIX SUBSTRATE
16
GATE
15
SOURCE
DRAIN
19
19
19
19
C_{LC1}
C_{LC2}
C_{LC3}
C_{LCn}
20
20
20
20
C_1
C_2
C_3
C_n
18
COMMON ELECTRODE SUBSTRATE
WITH CONTROL CAPACITORS

Fig. 3b

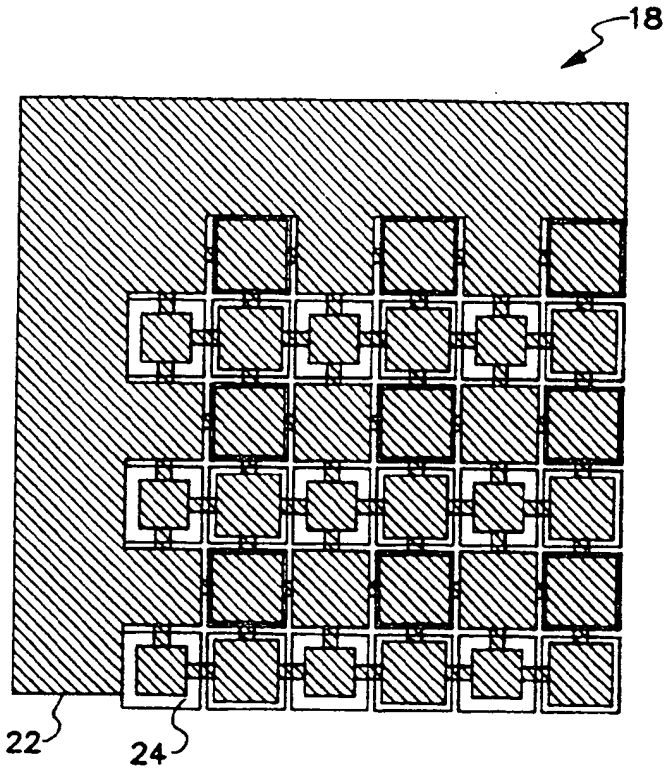

Fig. 4

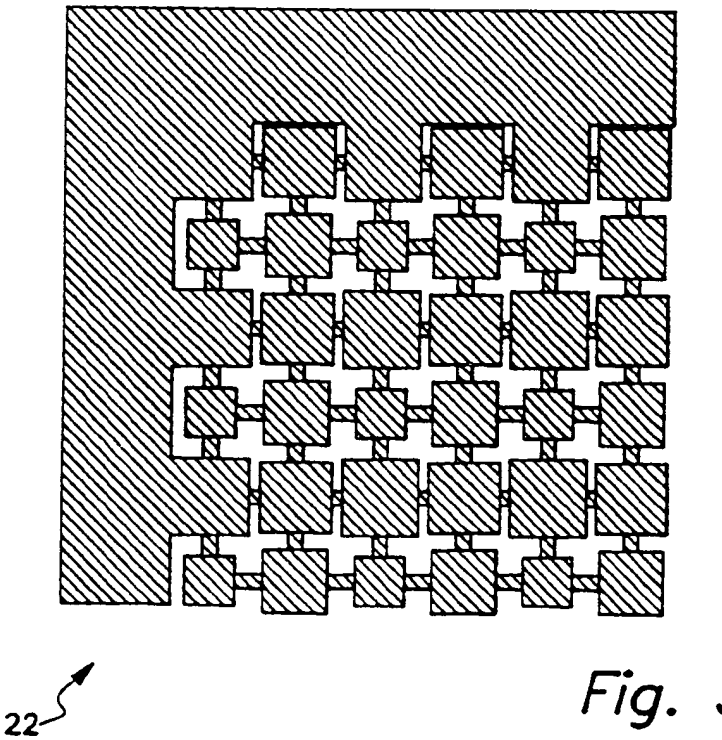

Fig. 5

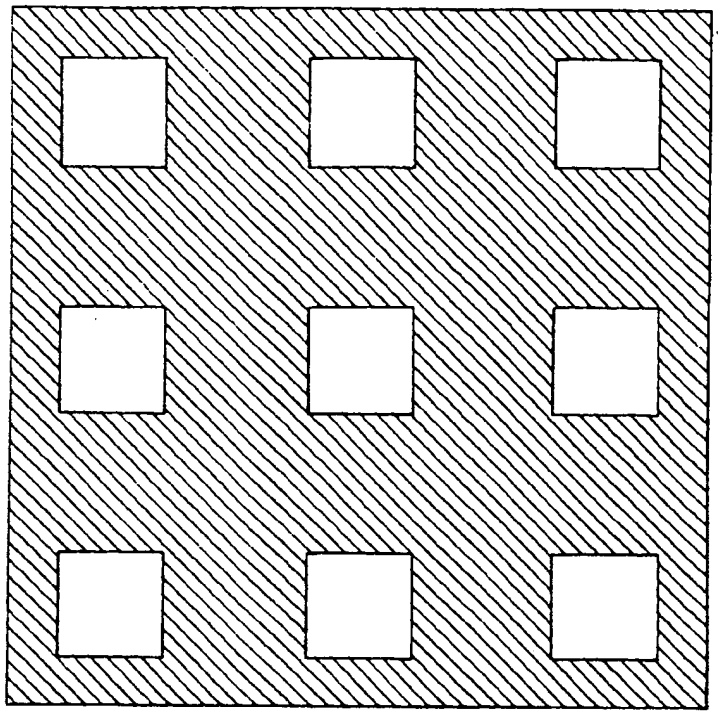

Fig. 6

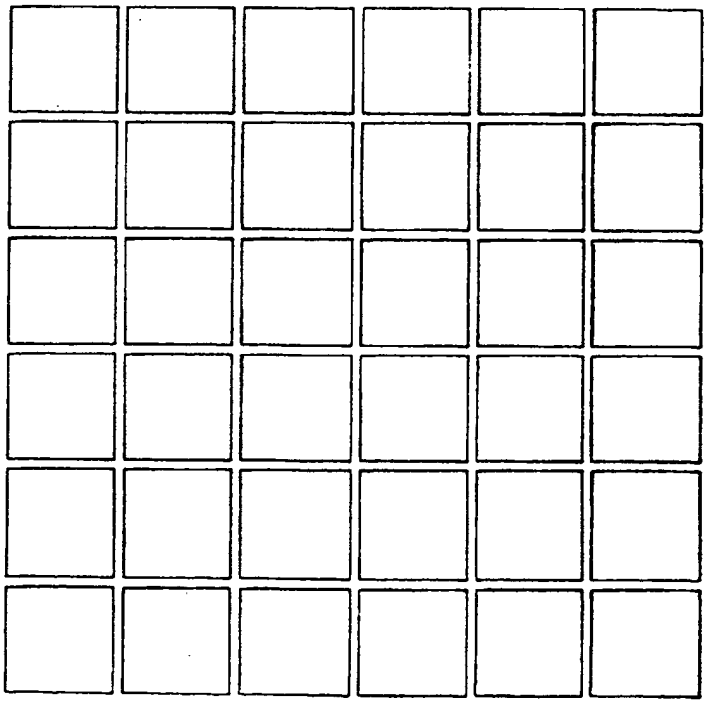

Fig. 7

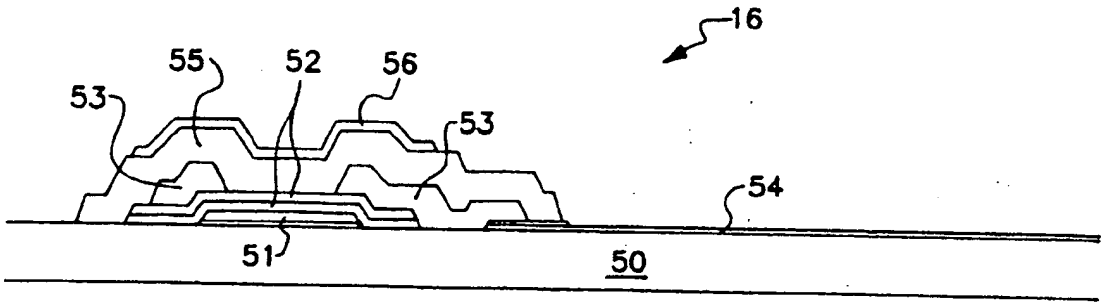

Fig. 8a

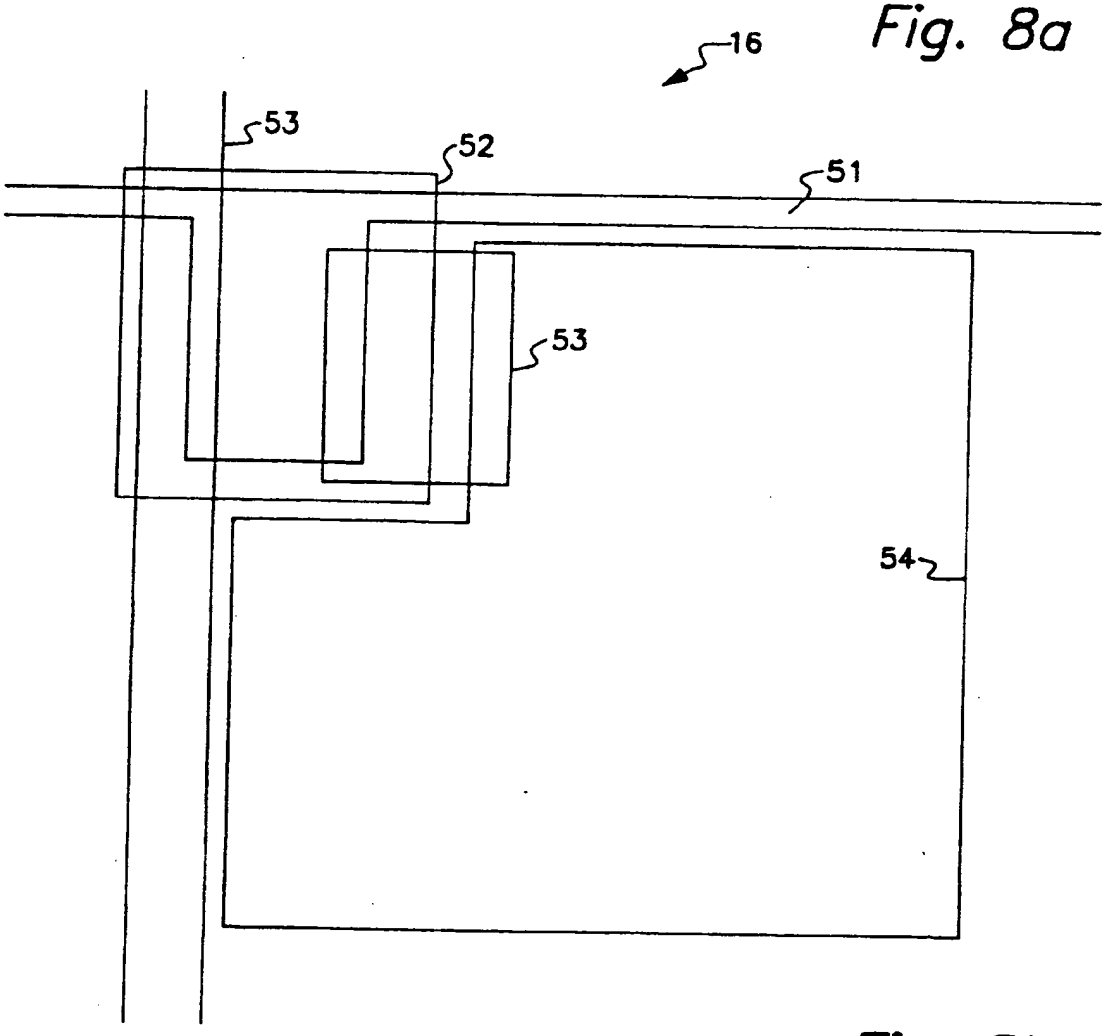

Fig. 8b

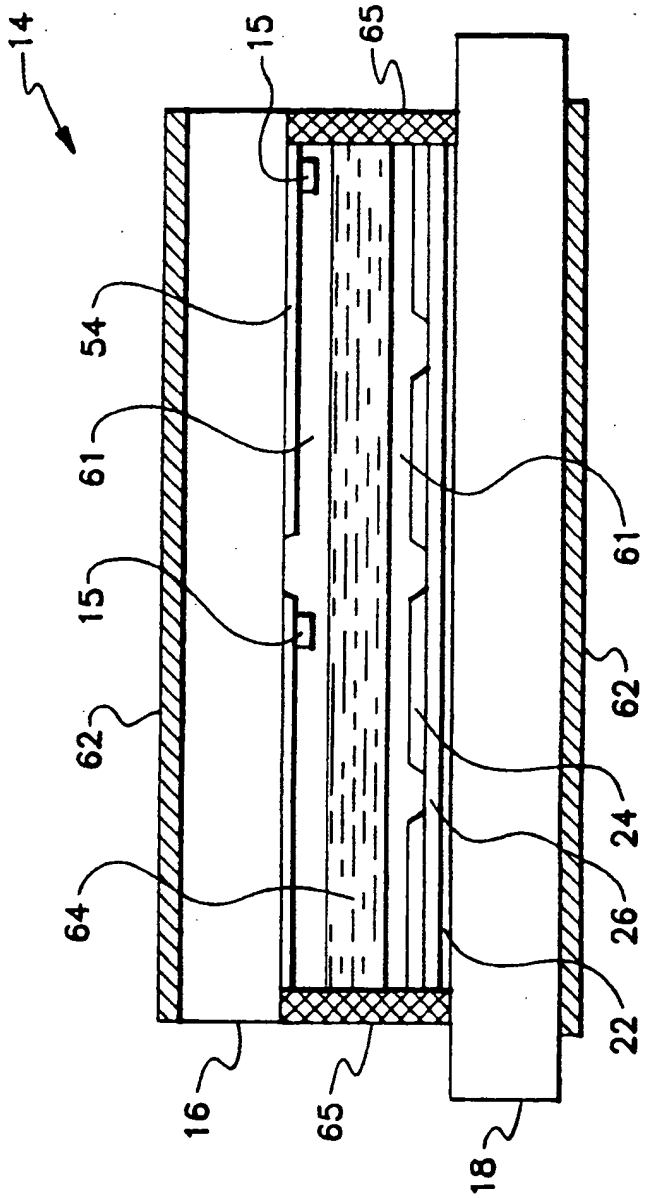

Fig. 9

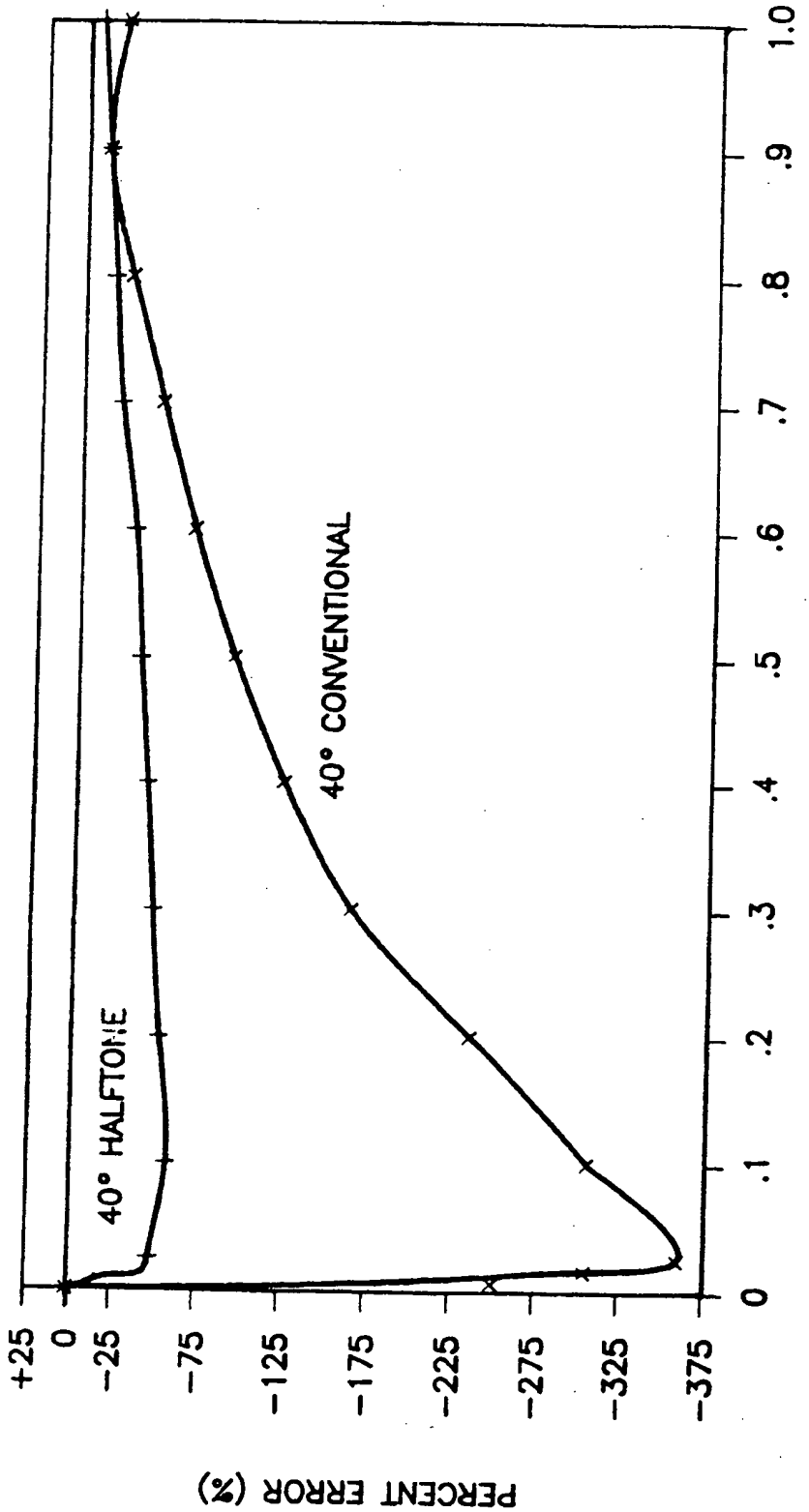
+25
0
-25
-75
-125
-175
-225
-275
-325
-375
PERCENT ERROR (%)
0
.1
.2
.3
.4
.5
.6
.7
.8
.9
1.0
GRAY LEVEL
40° HALFTONE
40° CONVENTIONAL

Fig. 10

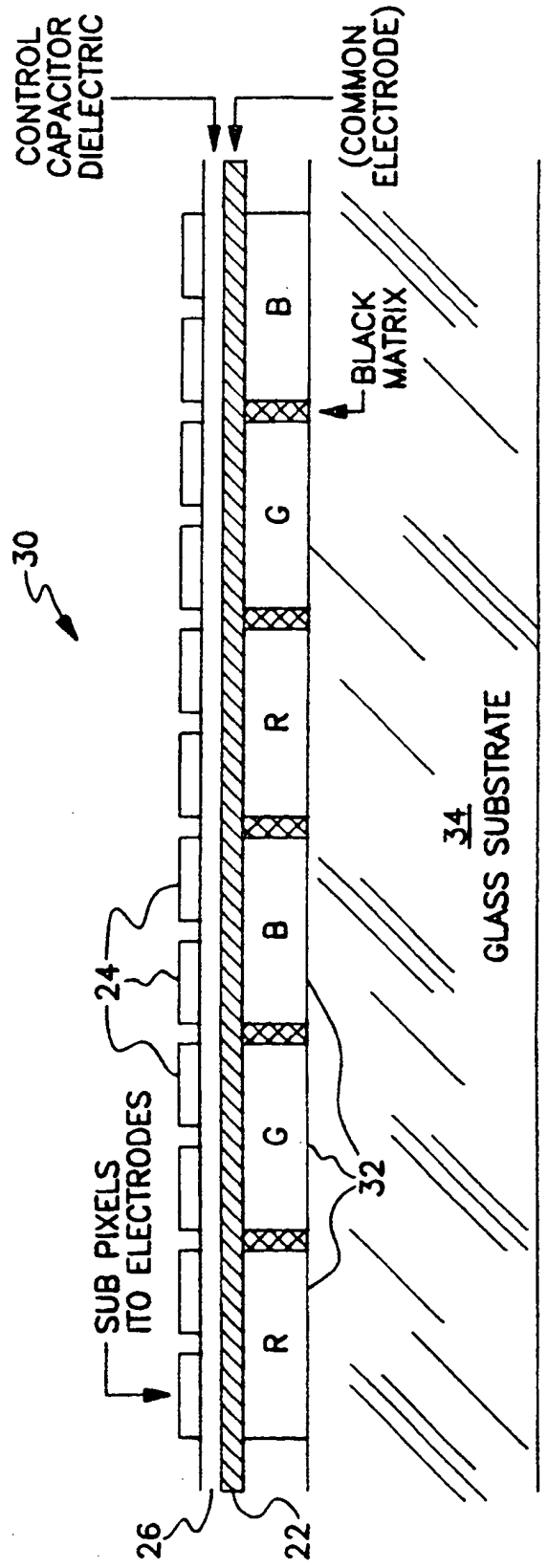
CONTROL CAPACITOR DIELECTRIC
(COMMON ELECTRODE)
BLACK MATRIX
30
B
G
R
B
G
R
24
SUB PIXELS ITO ELECTRODES
32
34
GLASS SUBSTRATE
26
22

Fig. 11

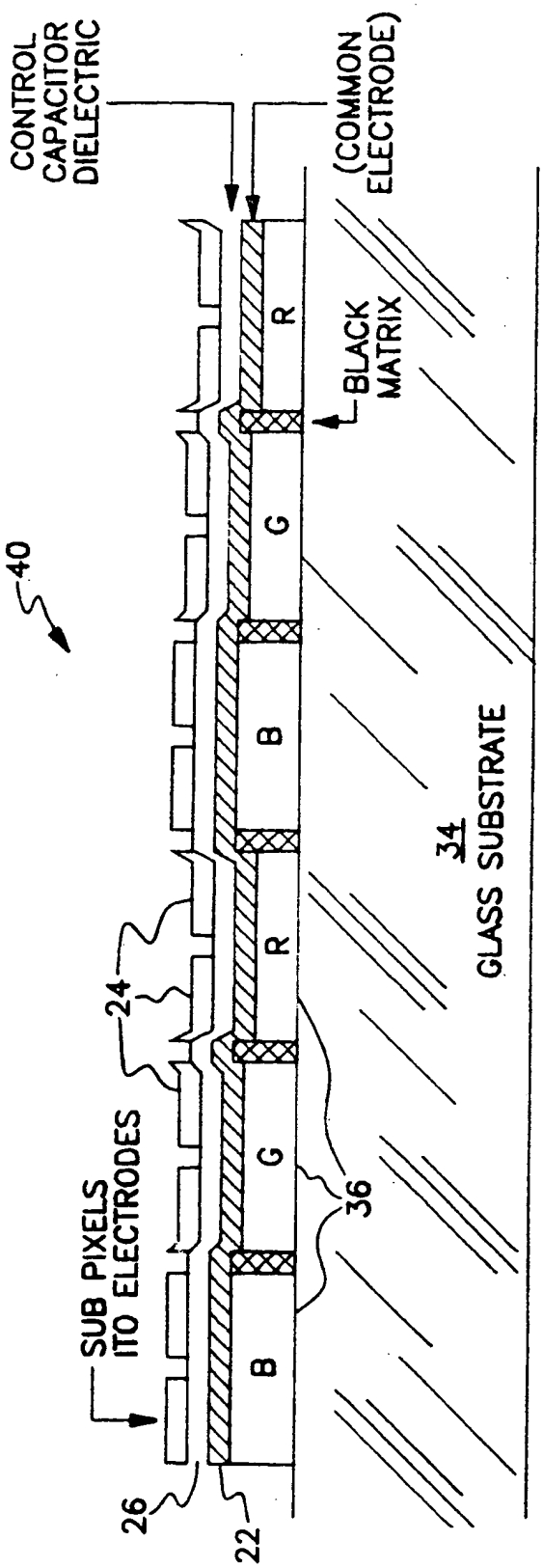
CONTROL CAPACITOR DIELECTRIC
(COMMON ELECTRODE)
BLACK MATRIX
40
R
G
B
R
G
B
24
36
SUB PIXELS ITO ELECTRODES
26
22
34
GLASS SUBSTRATE

Fig. 12

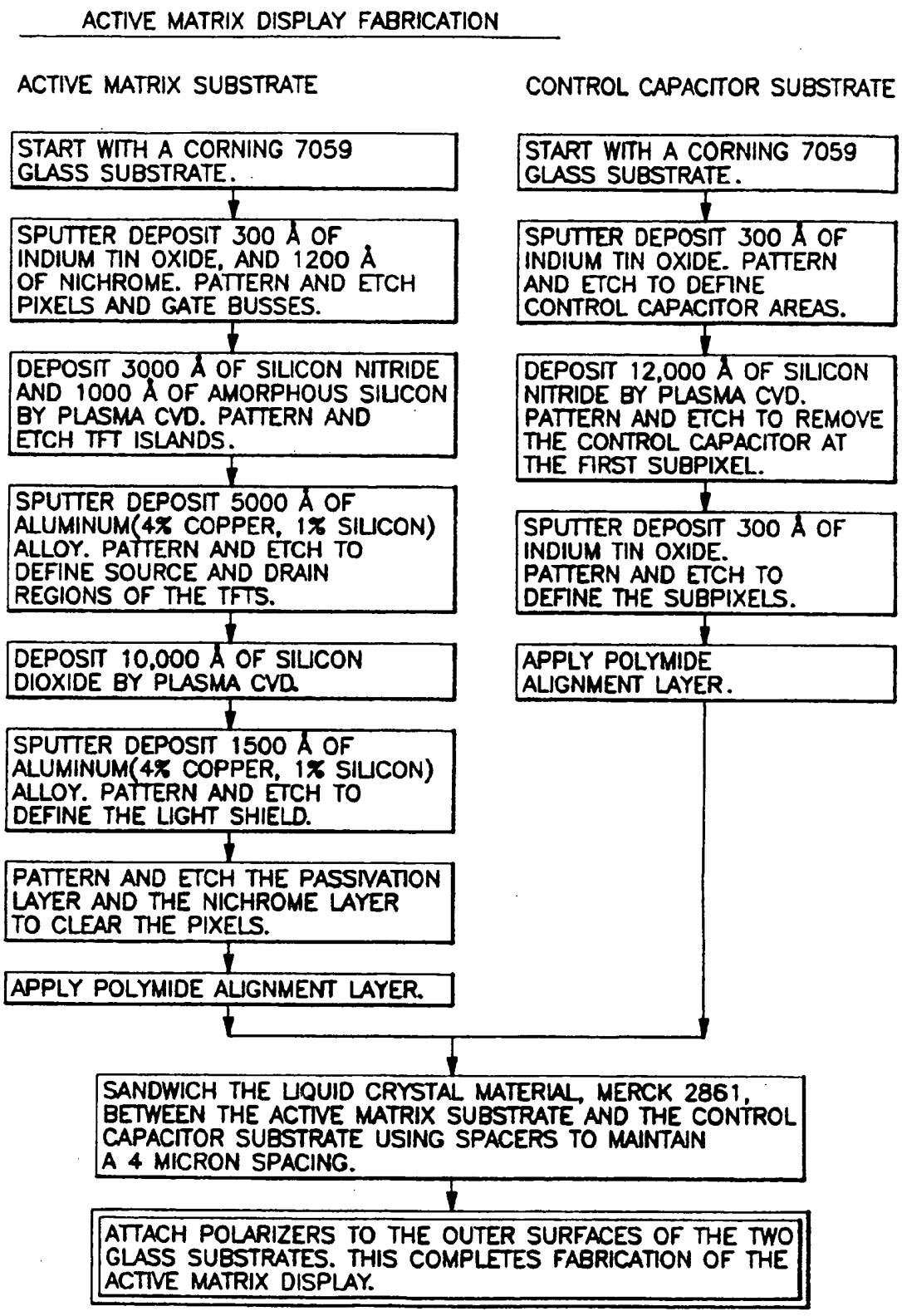
ACTIVE MATRIX DISPLAY FABRICATION
ACTIVE MATRIX SUBSTRATE
START WITH A CORNING 7059 GLASS SUBSTRATE.
SPUTTER DEPOSIT 300 Å OF INDIUM TIN OXIDE, AND 1200 Å OF NICHROME. PATTERN AND ETCH PIXELS AND GATE BUSSES.
DEPOSIT 3000 Å OF SILICON NITRIDE AND 1000 Å OF AMORPHOUS SILICON BY PLASMA CVD. PATTERN AND ETCH TFT ISLANDS.
SPUTTER DEPOSIT 5000 Å OF ALUMINUM(4% COPPER, 1% SILICON) ALLOY. PATTERN AND ETCH TO DEFINE SOURCE AND DRAIN REGIONS OF THE TFTS.
DEPOSIT 10,000 Å OF SILICON DIOXIDE BY PLASMA CVD.
SPUTTER DEPOSIT 1500 Å OF ALUMINUM(4% COPPER, 1% SILICON) ALLOY. PATTERN AND ETCH TO DEFINE THE LIGHT SHIELD.
PATTERN AND ETCH THE PASSIVATION LAYER AND THE NICHROME LAYER TO CLEAR THE PIXELS.
APPLY POLYMIDE ALIGNMENT LAYER.
CONTROL CAPACITOR SUBSTRATE
START WITH A CORNING 7059 GLASS SUBSTRATE.
SPUTTER DEPOSIT 300 Å OF INDIUM TIN OXIDE. PATTERN AND ETCH TO DEFINE CONTROL CAPACITOR AREAS.
DEPOSIT 12,000 Å OF SILICON NITRIDE BY PLASMA CVD. PATTERN AND ETCH TO REMOVE THE CONTROL CAPACITOR AT THE FIRST SUBPIXEL.
SPUTTER DEPOSIT 300 Å OF INDIUM TIN OXIDE. PATTERN AND ETCH TO DEFINE THE SUBPIXELS.
APPLY POLYMIDE ALIGNMENT LAYER.
SANDWICH THE LIQUID CRYSTAL MATERIAL, MERCK 2861, BETWEEN THE ACTIVE MATRIX SUBSTRATE AND THE CONTROL CAPACITOR SUBSTRATE USING SPACERS TO MAINTAIN A 4 MICRON SPACING.
ATTACH POLARIZERS TO THE OUTER SURFACES OF THE TWO GLASS SUBSTRATES. THIS COMPLETES FABRICATION OF THE ACTIVE MATRIX DISPLAY.

Fig. 13